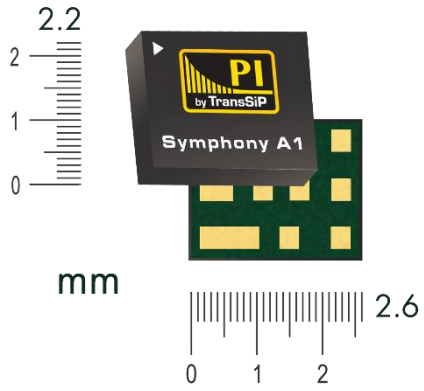
Symphony A1



Low-Noise Low-Jitter Buck Converter with SNJ Conditioning

Empower Noise-sensitive Applications:

- Energy Harvesting
- GPS / GNSS
- Audio and Video
- Wirelss
- IoT Devices
- Remote Control

*Note: Terms and conditions apply to all TransSiP products and solutions. The Terms are available at www.transsip.com

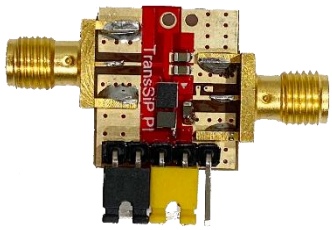
Revision History

1/2023	Revision 0.0 Preliminary Draft
9/2023	Revision 1.0 Preliminary Datasheet

Design Resources

Evaluation Kits

- Symphony A1 Evaluation Board



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Contents

1.0 Introduction

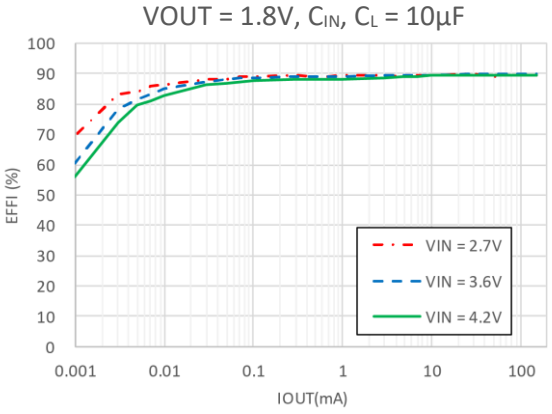
TransSiP PI solutions set a new standard in systems' performance based on the patented Switching Noise Jitter (SNJ) conditioning technology. Furthermore, the addition of the Symphony A1 DC-DC buck conversion chipset further empowers the TransSiP PI family to support low power and noise-sensitive SoCs down to 0.5V core voltage while enhancing systems' performance.

The Symphony A1 comprises of two functions in a single package – PFM Controller and SNJ Conditioner. With the best 200nA current consumption (Iq), 0 µA standby current, and high conversion efficiencies down to 1 µA light-load, the Symphony A1 can already enhance battery life better than the norm in the market. Furthermore, the dual selectable VOUT1 and VOUT2 feature helps lower the inventory management and logistic costs that one-part-number can use in multiple circuits.

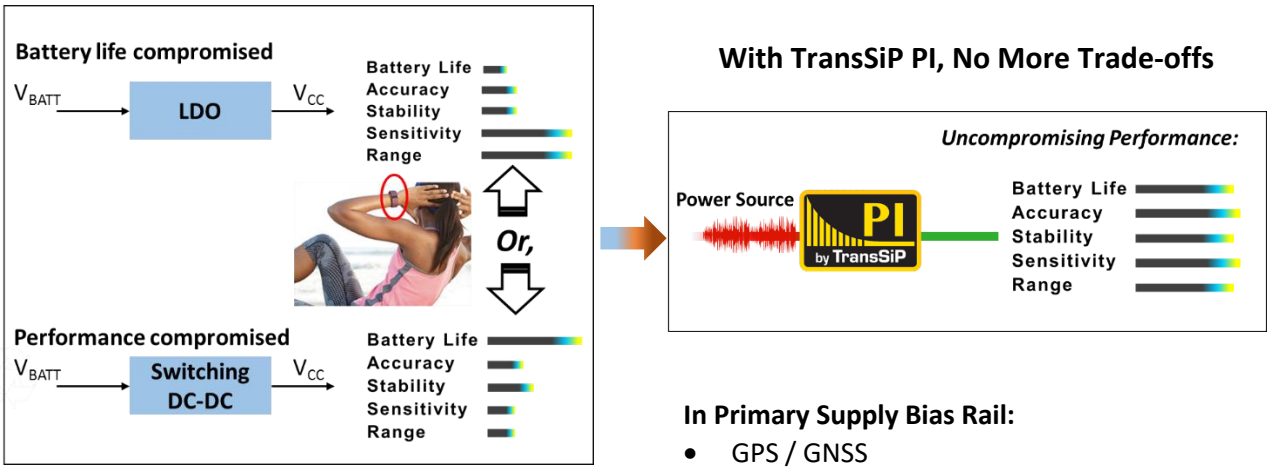
The Symphony A1 delivers an uncompromised system's performance equivalent to, if not better than, low-noise LDO for GPS/GNSS, wireless connectivities, and other noise-sensitive devices for longer battery life, higher accuracy, signal clarity, and reliability.

1.1 Key Features

Noise Elimination:	Patented SNJ Conditioning
Switching Mode:	PFM only (no modes switching noise commonly with PFM/PWM type)
Switchable Output Voltage:	Select VOUT 1 or VOUT 2 by VSEL Pin; reduce inventory and logistic costs
Low-Frequency Switching:	10 ~ 20 kHz (typ.)
Noise and Harmonics:	No switching noise and harmonics above 1MHz
Min. Input Voltage:	1.8 V (6.0Vmax)
Min. Output Voltage:	0.5 V (3.6Vmax; 0.05V increments)
Quiescent Current:	200 nA typ. (VOUT = 1.8V)
Output Current:	150 mA
Standby Current:	0.0 µA (typ.)
Protection:	UVLO Short Circuit Protection Input Voltage Bypass Rush Current Limit CL Discharge (option)
Operating Temperature:	-40°C to +85°C
Compliance:	RoHS
Package:	2.2 x 2.6 x 0.9 [mm]



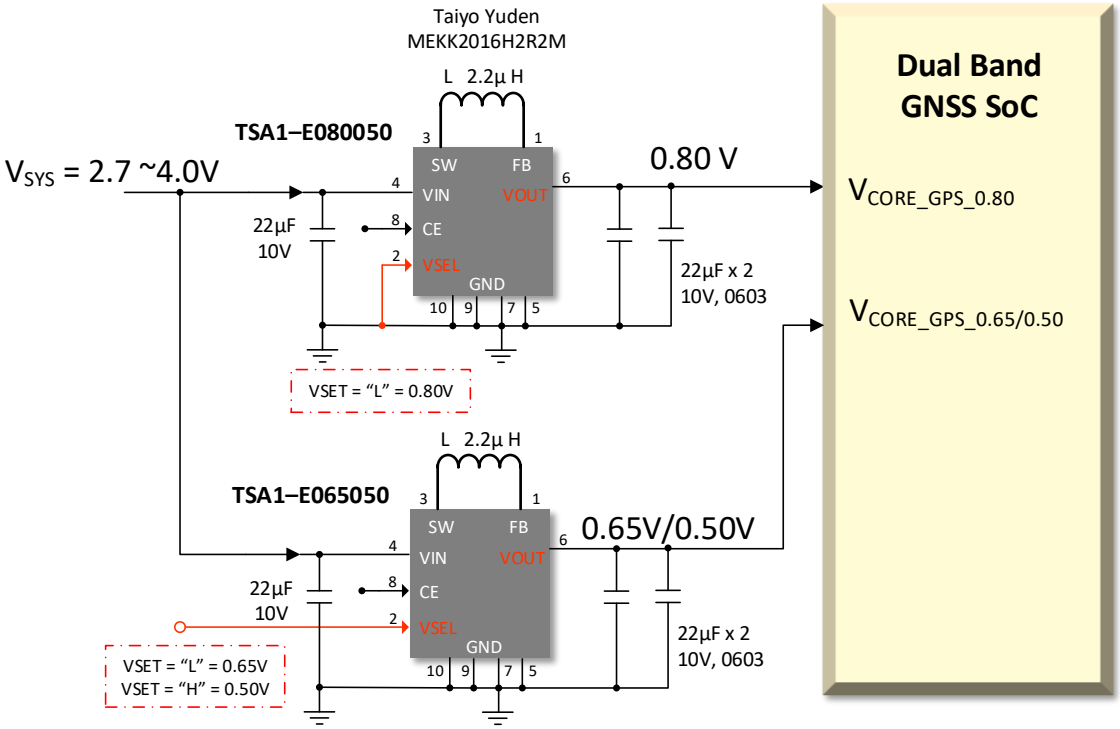
1.2 TransSiP PI Advantages and Applications



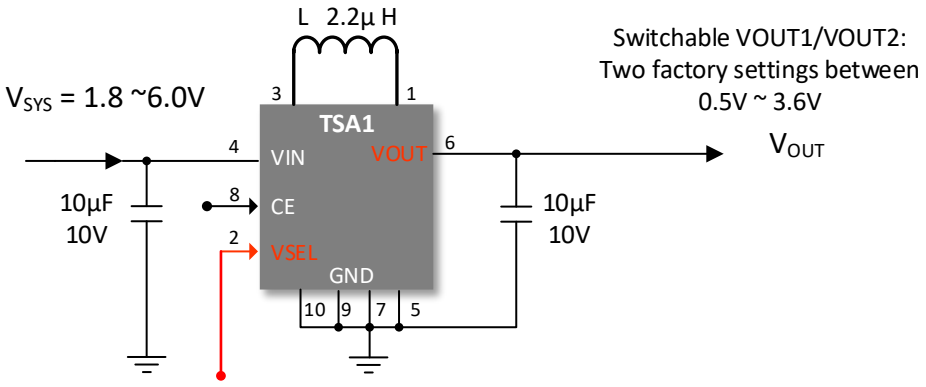
In Primary Supply Bias Rail:

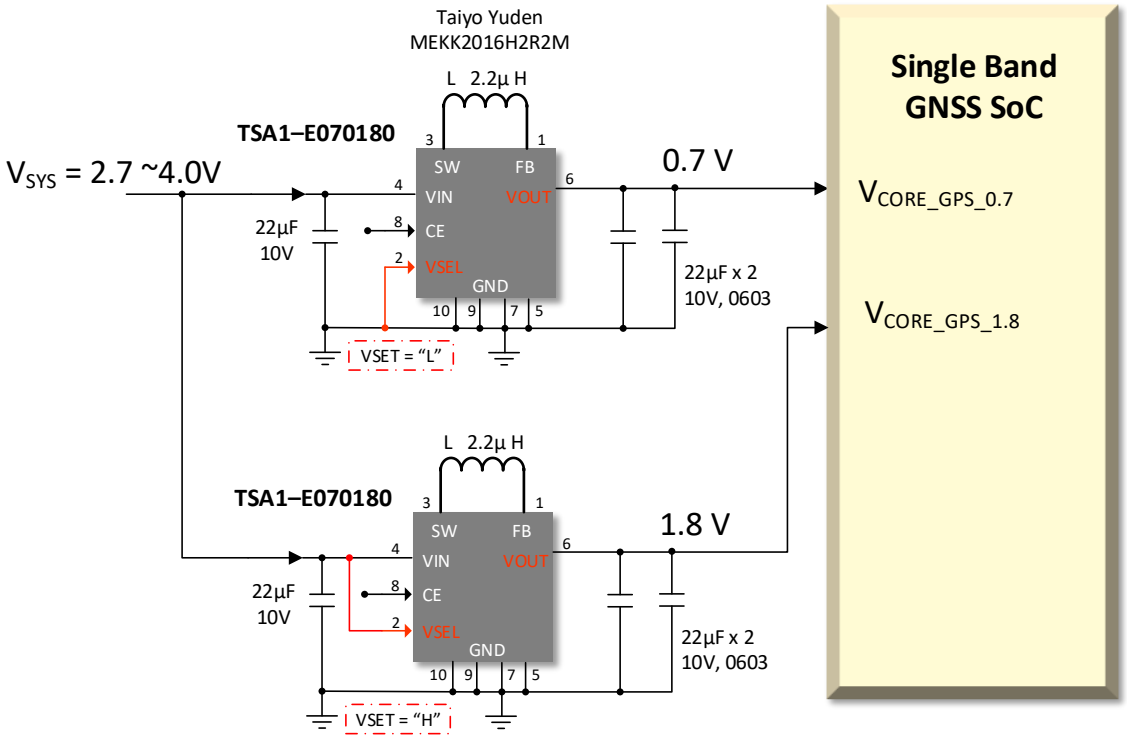
- GPS / GNSS
- High Precision Clocks
- Optical HR and Biomedical Sensors
- Geophones
- Audio and Video Applications
- Hearing Aid
- Solid State Disks and Memories
- High Speed Digital Systems

1.3 Example for Ultra-low Power Dual Band GNSS SoC



1.4 General Applications of the Symphony A1 and Single Band GNSS SoC





2.0 Technical Description

The Symphony A1 comprises an ultra-low-power step-down PFM Controller and a Switching Noise Jitter (SNJ) Conditioner. The A1 architecture is a revolutionary patented JC-PFM™ circuit topology for a noise-optimized and SNJ-free switched-mode DC-DC converter. The topology solves the most difficult and unresolved problem in the electronics industry for DC-DC conversion – Noise.

The advantage is to enable a single-mode PFM operation to deliver high conversion efficiency throughout the entire load range without conventional PFM operation's chaotic noise. Another advantage of single-mode PFM operation is eliminating the problematic transient noise incurring with dual-mode switching, for instance, PFM-PWM type, in which the additional mode switching noise is detrimental to noise-sensitive applications.

The SNJ conditioner enables a noise-optimized and SNJ-free feedback signal in the PFM controller feedback control loop. In addition, it makes the JC-PFM circuit topology suitable to replace LDO and conventional switched-mode DC-DC buck converters, thereby eliminating the tradeoffs between systems performance and power conversion efficiency in noise-sensitive applications.

Low-frequency switching is another prominent feature of the Symphony A1. No switching harmonics exist beyond 1MHz, even with a noisy DC power source such as energy harvesting, AC-DC converters, or others. The A1 consumes 200nA quiescent current (typ @ Vout = 1.8V) and provides high conversion efficiency even at 1uA light-load. The operating voltage (V_{IN}) of the A1 is as low as 1.8V.

Lowering inventory management and logistic costs is another advantage of the chipset. Enabled by state-of-the-art 0.0 µA standby current and two factory pre-selected VOUT1 and VOUT2 between 0.5V to 3.6V, the features enable one part number to use in multiple circuits.

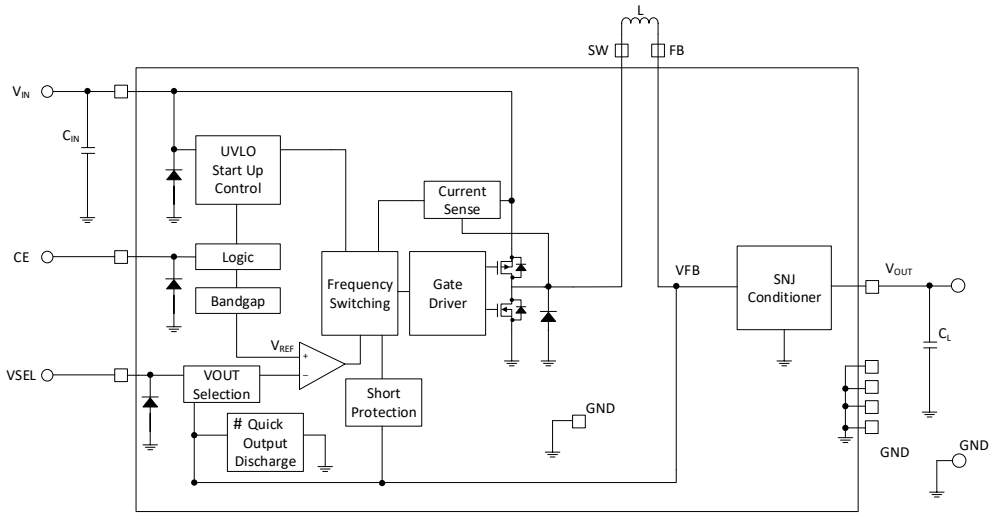
Other key features include quick output discharge, short protection, rush current limit, and input undervoltage lockout (UVLO). The A1 chip is in LGA of 2.2 mm x 2.6 mm x 0.9 mm.

2.1 Ordering Part Numbers and Factory Programmable Options

Symphony A1 PN TSA1-①②③④⑤⑥⑦	**FEATURE**	**SYMBOL**	**DESCRIPTION**
①	Quick Output Discharge	E / D	E = Enabled, D = Disabled
②③④	Output Voltage 1 (VOUT1)	0 – 9	Range: 0.60V ~ 3.60V (0.05V step) e.g. Vout = 0.70V → ②③④ = 070
⑤⑥⑦	Output Voltage 2 (VOUT2)	0 – 9	Range*: 0.50V ~ 3.60V (0.05V step) e.g. Vout = 1.80V → ④⑤⑥ = 180
*Note: VOUT1 < VOUT2 except when VOUT2 = 0.50V, for examples: TSA1-E080180 = Quick Output Discharge Enabled, VOUT1 = 0.80V, VOUT2 = 1.80V TSA1-E065050 = Quick Output Discharge Enabled, VOUT1 = 0.65V, VOUT2 = 0.50V			

Standard PN:	**Laser Mark Identifier**
TSA1-E065050	A1001E
TSA1-E080050	A1R16E
TSA1-E070180	A1141E
TSA1-E080180	A1254E
TSA1-E100180	A1468E
TSA1-E180300	A1B90E

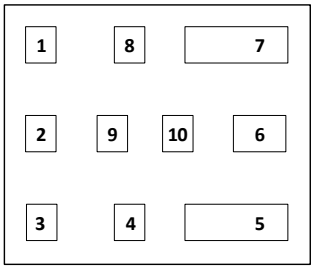
2.2 Block Diagram



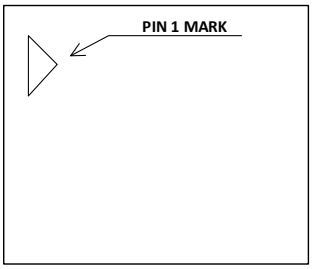
Optional factory programmable feature. TSA1-E = Enabled; TSA1-D = Disabled

2.3 Pin Assignment and Package Type

(Top View)



(Top View)



TSA1 LGA-2226	Pin Name	Function
1	FB	Feedback Node
2	VSEL	Switchable VOUT Selection
3	SW	Switching Node
4	VIN	Power Source
5	GND	Ground
6	VOUT	SNJ Conditioned Output
7	GND	Ground
8	CE	Chip Enable
9	GND	Ground
10	GND	Ground

Function	Signal	Status
CE	L	Standby
	H	Active
VSEL	L	VOUT 1
	H	VOUT 2

Notes: Do not leave the VSEL pin open
Standard configuration is VOUT 1 < VOUT 2, but except when VOUT 2 = 0.50V

2.4 Absolute Maximum Ratings

TSA1 Parameter	Rating
VIN to GND	-0.3 V to +7 V
SW to GND	-0.3V to V_{IN}+0.3 V or +7V *
VOUT to GND	-0.3V to V_{IN}+0.3 V or +7V *
FB to GND	-0.3V to V_{IN}+0.3 V or +7V *
CE to GND	-0.3 V to +7 V
VSEL to GND	-0.3 V to +7 V
Storage Temperature Range	-55°C to +125°C
Operational Ambient Temperature	-40°C to +85°C

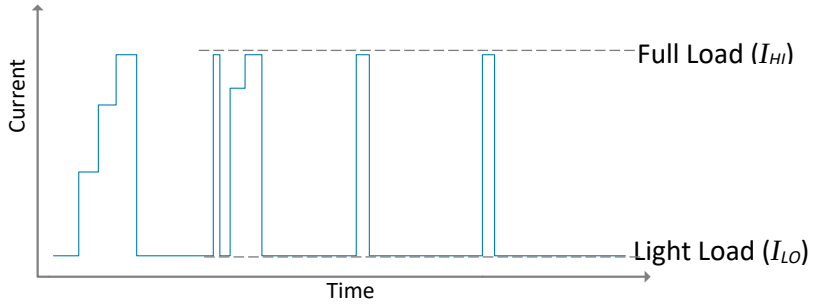
* The maximum value is the lower of either V_{IN} + 0.3V or +7V

2.5 Supply Bias Noise Primer for Switching-Noise-Jitter (SNJ) Conditioning

2.5.1 Background

Many modern wireless, mixed signals, and digital SoCs and subsystems operate in complex power-saving modes collectively described as pulsed applications as shown in Fig. 1 below (i.e. current drain fluctuates in pulses). Typically, a load enters a high-power state (e.g. RX/TX On or data lines active) for tens of micro- to milli-seconds and is then switched to low power or standby mode for hundreds of milli- to tens of seconds. The transient fluctuation of the load current induces perturbation of noise events in the feedback control loop circuitry of DC-DC converters.

FIG. 1 Current draw profile of load utilizing power saving modes (i.e. Pulsed Applications)



Some critical, high speed and noise-sensitive functions inside the SOCs and subsystems are vulnerable to this transient fluctuation, for example, precision calibrated “keep alive” clock, frequency drift of TCXO at wake-up, and analog-to-digital converter. Low noise supply bias and power integrity are still required by these circuits during the transitions between different power modes in order to maintain systems performance consistency during wake-up and transitions between these complex power-saving modes.

At present, modern switching DC-DC converters offer dual-mode or power-saving operation by fixing the switching frequency (e.g. PWM) at full-load, thereby easing LC filtering and ripple voltage reduction at “full-load”. When light-loads are present, they switch to power-saving mode, typically referred to as pulse-frequency, pulse-skipping or hysteresis or frequency-reduction mode for increased efficiency, however in the process incurring higher ripple voltage and transient noise at “light-loads” and “light-to-full-loads transition” or vice versa. Nevertheless, it is vital to consider the overall probability and noise profile of dual-mode operation to really understand the impact of noise and savings in powering pulsed applications. As

illustrated in Fig. 1 (not to scale), the probability of full-load operation can be 0.05 (5%) or smaller, which means at least 95% of the time, the supply bias will present high ripple-voltage as well as transient and wide-spectrum noise even with dual-mode operation. Also, the switching from light-load to full-load must be fast. This has the effect of creating additional transient noise and momentary fluctuations in output voltage, as well as reduced efficiency due to increased quiescent current as required by complex mode-switching circuitry.

2.5.2 Observation and Measurement of SNJ

Switching noise jitter (SNJ) can occur in switching regulators as the perturbation of noise causes dislocation in upslope ($T_{ON\_PFM+NOISE}$) and downslope ($T_{OFF\_PFM+NOISE}$) timing of the sawtooth ripple waveform produced by switched-mode power supplies (SMPS). The ripple waveform exhibits jitter, and, as shown in Fig. 2, noise carried on the ripple perturbates. The noise perturbation (SNJ) is present in the time-domain on the output-voltage shown in Fig. 3. The observation of SNJ is not on the peak-to-peak ripple-voltage or amplitude of spectral noise density, but the SNJ signature in the time-domain. Since the Symphony A1 is PFM type, the switching frequency always moves on the oscilloscope with the load transients. Thus, it is impossible to determine which movement of the waveform in T_{ON_PFM} and T_{OFF_PFM} is caused by the load transients or the perturbation of noise in the control loop circuitry. To address this problem, a new measurement method was developed by TransSiP based on the Tektronix DPX® Spectrum display provided by the Tektronix RSA306 real time spectrum analyzer. The example in Fig. 3 illustrates the SNJ signature as a measurement in noise perturbation density and is expressed as a percentage.

FIG. 2 Output-voltage Ripple with the Present of SNJ

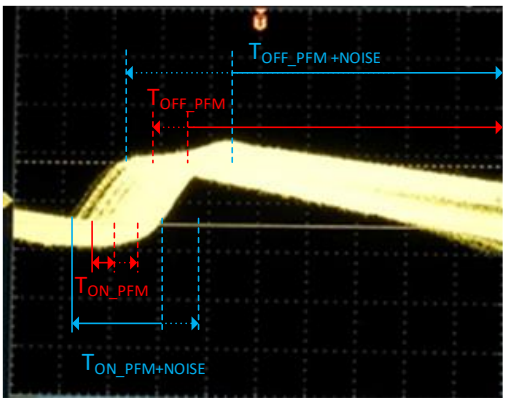
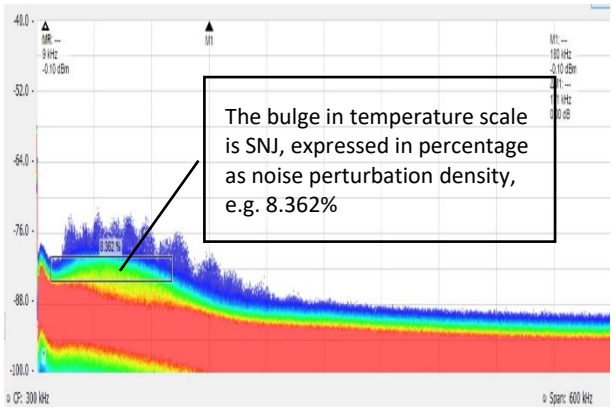


FIG. 3 SNJ Measurement by DPX



2.5.3 The Influence of SNJ

The influence of SNJ is accumulative in many modern digital and mixed signals systems, creating an aggregation of perturbated signals over time which will degrade the quality of signal convolution and the resulting digital mapping into memory. Furthermore, the presence of SNJ on the supply bias exacerbates the impact on some critical, high speed, and noise-sensitive functions inside SOCs and subsystems which are vulnerable to this extra degree of noise, for example, precision calibrated keep alive clock, frequency drift of TCXO at wake-up and ADC.

The magnitude of SNJ is neither dependent on the magnitude of output-ripple voltage nor on the spectral noise density measured in nV/√Hz. Reduction of output-ripple voltage or spectral noise density does not eliminate SNJ on the supply bias. In fact, SNJ becomes a dominating influence on the performance of many modern noise-sensitive SoCs and circuit components after the output-ripple voltage or spectral noise density on supply bias has been suppressed.

2.5.4 The Significance of SNJ Conditioned DC-DC Conversion

The patented JC-PFM topology eliminates the unwanted SNJ signature directly observable on the output-voltage ripple or as noise perturbation density shown in Figs. 4 and 5. In comparison to Fig. 3 above, the noise perturbation density has been reduced by over 50%: the remaining peaks are associated with the continued presence of residual ripple on the output supply bias. The JC-PFM topology of the Symphony A1, therefore, not only provides a best-in-class noise profile in pulsed applications but is also highly effective in noise-sensitive light-load applications: enabling downstream circuit performance equivalent to if not better than identical systems powered by low-noise LDO regulation, and better than anything that has been encountered with non-SNJ conditioned switched-mode DC-DC regulation. That is because the SNJ conditioner reduces the noise perturbation in the feedback signal to the Controller, thereby ensuring optimal noise profile on the supply bias for noise-sensitive applications.

FIG. 4 Output-voltage Ripple after SNJ Conditioning

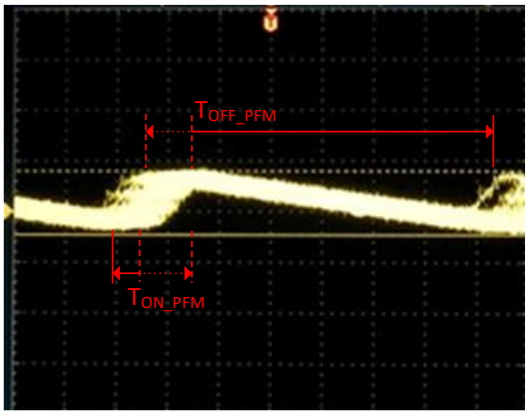
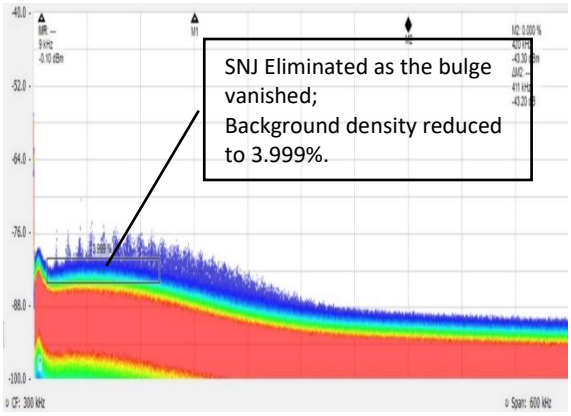


FIG. 5 DPX Plot of SNJ-Conditioned Supply Bias



2.6 Electrical Characteristics

TSB2-xxxx, Ta = 25°C

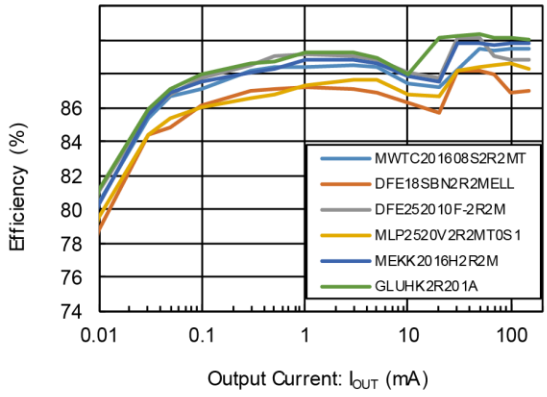
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Input Supply Voltage Range	V_{IN}	1.8		6.0	V	
Output Voltage Range	V_{OUT}	0.50		3.60	V	Factory Programmable (0.05V step)
Output Current	I_{OUT}	150			mA	
Standby Current	I_{STBY}		0.0	0.1	µA	V_{IN} = 6V, V_{CE} = V_{OUT} = 0V
Quiescent Current	I_q		200	750	nA	V_{OUT} ≤ 1.30V, V_{IN} = V_{CE} = 1.8V, VSEL= 0V V_{OUT} ≥ 1.40V, V_{IN} = V_{CE} = V_{OUT} +0.5V, VSEL= 0V
UVLO Detect Voltage	V_{UVLOD}		1.50	1.78	V	Across operating temperature
UVLO Release Voltage	V_{UVLOR}	1.00	1.40		V	Across operating temperature
Switching Frequency	F_{SW}	10	20	600	kHz	
CE and VSEL Pin Input Voltage Threshold High Low Input Leakage Current	 V_{CEH} V_{CEL} I_{CE_Leak}	 1.2 GND	 0.0	 6.0 0.3 0.1	 V V µA	 V_{SEL_H} for the VSEL Pin V_{SEL_L} for the VSEL Pin
PFM Switching Current	I_{PFM}		400	600	mA	V_{IN} = V_{OUT} + 2V, I_{OUT} = 10 mA
Efficiency	E_{ff}		94 94 90 84 82 78 77		%	V_{IN}=5.0V, V_{OUT}=3.0V, I_{OUT}=30 mA V_{IN}=4.2V, V_{OUT}=3.0V, I_{OUT}=30 mA V_{IN}=3.6V, V_{OUT}=1.8V, I_{OUT}=30 mA V_{IN}=1.8V, V_{OUT}=1.2V, I_{OUT}=30 mA V_{IN}=1.8V, V_{OUT}=1.0V, I_{OUT}=30 mA V_{IN}=1.8V, V_{OUT}=0.7V, I_{OUT}=30 mA V_{IN}=1.8V, V_{OUT}=0.5V, I_{OUT}=30 mA
SW Pin ON Resistance High-side Power FET Low-side Power FET	 R_{DS_H} R_{DS_L}		 0.35 0.32	 0.45 0.42	 Ω Ω	
Quick Output Discharge Resistance	R_{DIS}	29	45	60	Ω	Varies with V_{IN}
Short Protection Threshold	V_{SHORT}	0.1	0.5	0.8	V	VSEL = 5V SW pin voltage falling while V_{OUT} → 0V
Output Voltage Temperature Characteristics	ΔV_{OUT}		±100		ppm/°C	I_{OUT}=30 mA Across operating temperature

ESD CAUTION	
	ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

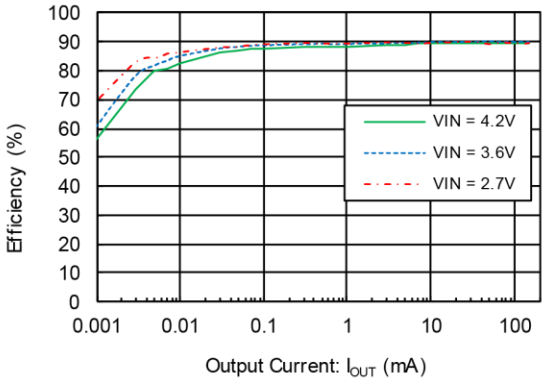
2.7 Typical Performance Characteristics

Ta = 25°C

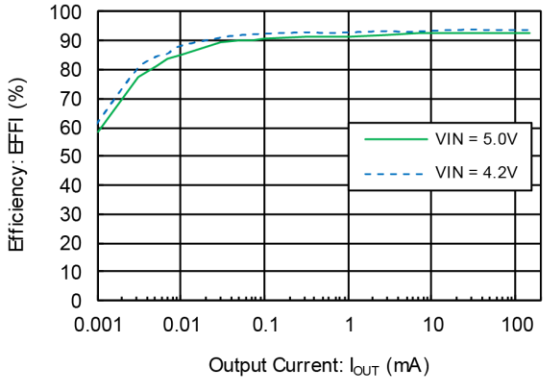
VIN = 3.6V, VOUT = 1.8V
CIN = 10µF, 10V
CL = (22µF, 6.3V) X 2



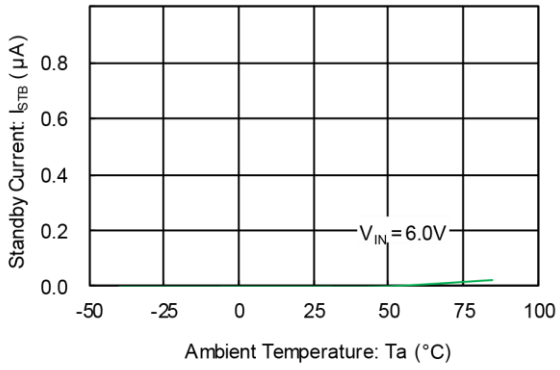
VOUT = 1.8V
L = GLUHK2R201A(2.2µH)
CIN = 10µF, 10V



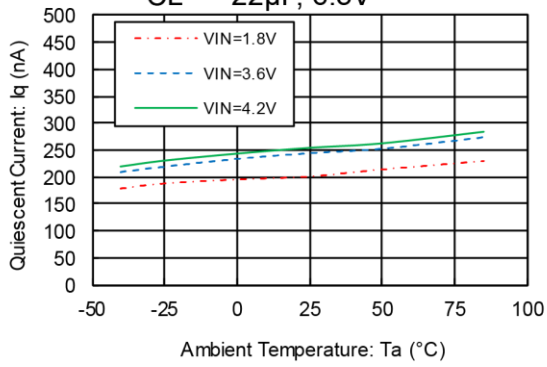
VOUT = 3.0V
L = GLUHK2R201A(2.2µH)
CIN = 10µF, 10V



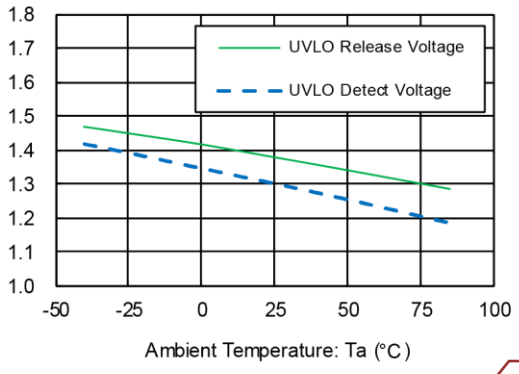
Standby Current vs. Ambient Temperature



VOUT = 1.8V
L = GLUHK2R201A(2.2µH)
CIN = 10µF, 10V
CL = 22µF, 6.3V



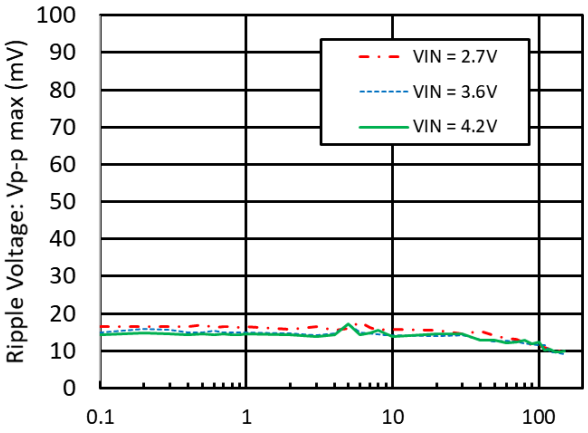
UVLO Voltage vs. Ambient Temperature



Ripple Voltage vs. Output Current

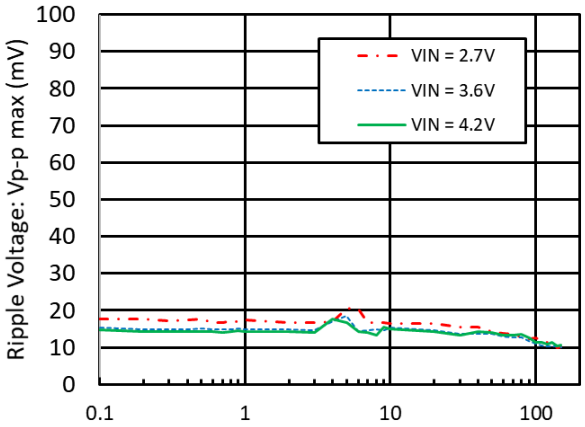
TSA1-E065050 (V_{OUT} = 0.50V)

L = MEKK2016H2R2M (2.2 µH)
C_{IN} = LMK107BBJ226MA-T (22 µF/10V)
C_{OUT} = LMK107BBJ226MA-T (22 µF/10V) x 2



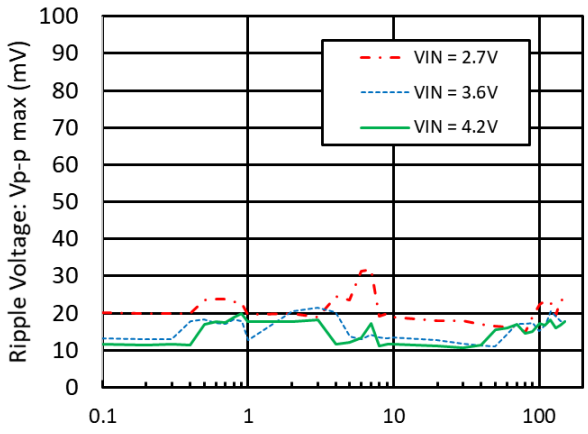
TSA1-E070180 (V_{OUT} = 0.70V)

L = MEKK2016H2R2M (2.2 µH)
C_{IN} = LMK107BBJ226MA-T (22 µF/10V)
C_{OUT} = LMK107BBJ226MA-T (22 µF/10V) x 2



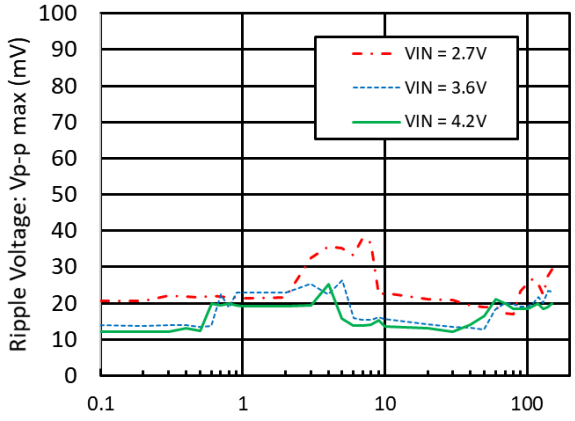
TSA1-E080180 (V_{OUT} = 1.80V)

L = MEKK2016H2R2M (2.2 µH)
C_{IN} = LMK107BBJ226MA-T (22 µF/10V)
C_{OUT} = LMK107BBJ226MA-T (22 µF/10V) x 2



TSA1-E070180 (V_{OUT} = 1.80V)

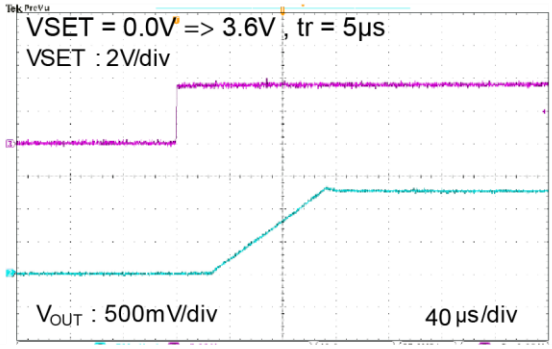
L = MEKK2016H2R2M (2.2 µH)
C_{IN} = LMK107BBJ226MA-T (22 µF/10V)
C_{OUT} = LMK107BBJ226MA-T (22 µF/10V) x 2



Switchable Output Voltage Function

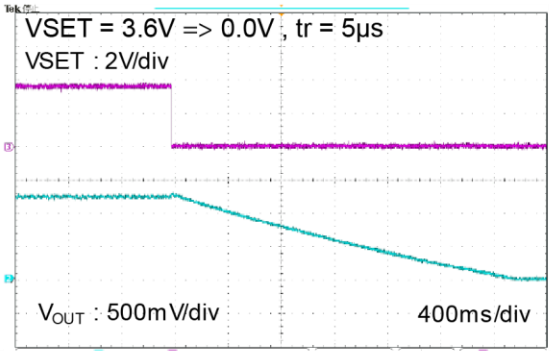
VIN = 3.6V, VOUT = 1.8V => 3.0V,
I_{OUT} = 10μA

L = GLUHK2R201A(2.2μH)
CIN = 10μF, 10V
CL = (22μF, 6.3V) x 2



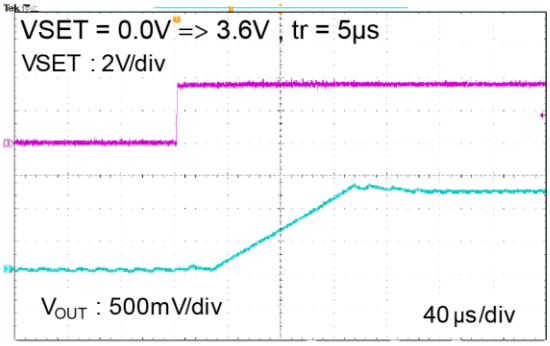
VIN = 3.6V, VOUT = 3.0V => 1.8V,
I_{OUT} = 10μA

L = GLUHK2R201A(2.2μH)
CIN = 10μF, 10V
CL = (22μF, 6.3V) x 2



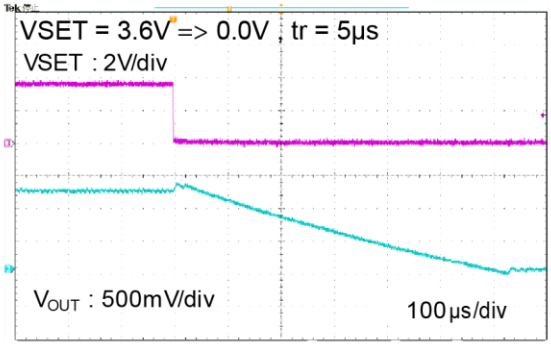
VIN = 3.6V, VOUT = 1.8V => 3.0V,
I_{OUT} = 50mA

L = GLUHK2R201A(2.2μH)
CIN = 10μF, 10V
CL = (22μF, 6.3V) x 2



VIN = 3.6V, VOUT = 3.0V => 1.8V,
I_{OUT} = 50mA

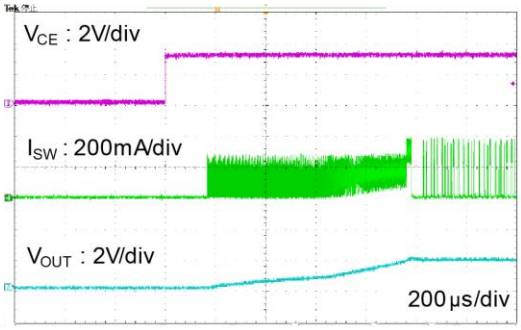
L = GLUHK2R201A(2.2μH)
CIN = 10μF, 10V
CL = (22μF, 6.3V) x 2



Startup Mode

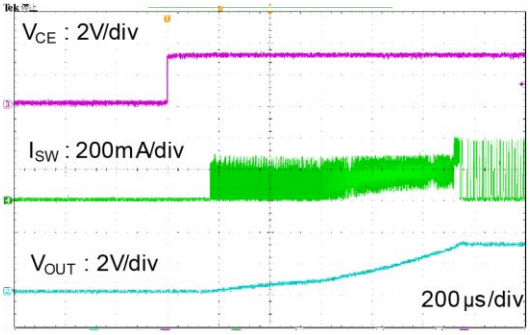
VIN = 3.6V, VOUT = 1.8V
VCE = 0.0V => 3.6V
I_{OUT} = 50mA

L = GLUHK2R201A(2.2μH)
CIN = 10μF, 10V
CL = (22μF, 6.3V) x 2



VIN = 3.6V, VOUT = 3.0V
VCE = 0.0V => 3.6V
I_{OUT} = 50mA

L = GLUHK2R201A(2.2μH)
CIN = 10μF, 10V
CL = (22μF, 6.3V) x 2



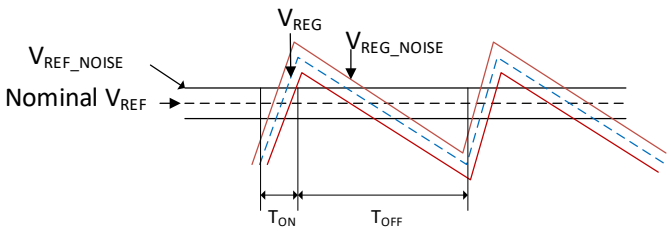
3.0 Feature Description

3.1 Overview

The significance of the Symphony A1 is its ability to deliver unparalleled efficiency, accuracy and performance to the wireless, mixed signals and digital SoCs that it powers. Featured with SNJ conditioning, the A1 chip ensures optimum supply bias quality under both full-load and light-load operating conditions while effectively converting DC voltage from a large variety of DC energy sources to levels required by noise-sensitive low-voltage FD-SOI, FinFET, and RF BiCMOS SOCs. The chipset features a wide input voltage range of 1.8V to 6.0V and delivers a high-quality output voltage switchable between two pre-selected VOUT 1 and VOUT 2 from 0.5V to 3.6V in increments of 0.05V.

3.2 JC-PFM Control

The PFM Controller operates at variable frequencies typically less than 20kHz in response to load fluctuation. When the high-side MOSFET switch turns on (T_{ON}) at the start of each oscillator cycle, an upslope voltage V_{REG} climbs up until feedback voltage V_{FB} is higher than V_{REF} or the current that flows through the high-side MOSFET switch reaches the Controller's defined switching current threshold (I_{JC-PFM}). Then the high-side MOSFET switch turns off (T_{OFF}) and the low-side MOSFET switch turns on. The on-time T_{ON} (off-time T_{OFF}) of the low-side MOSFET is dynamically optimized inside the PFM Controller. During the high-side MOSFET off time, the V_{REG} descends as a downslope voltage until it is lower than the V_{REF}, then the high-side MOSFET turns on again to begin a new cycle.



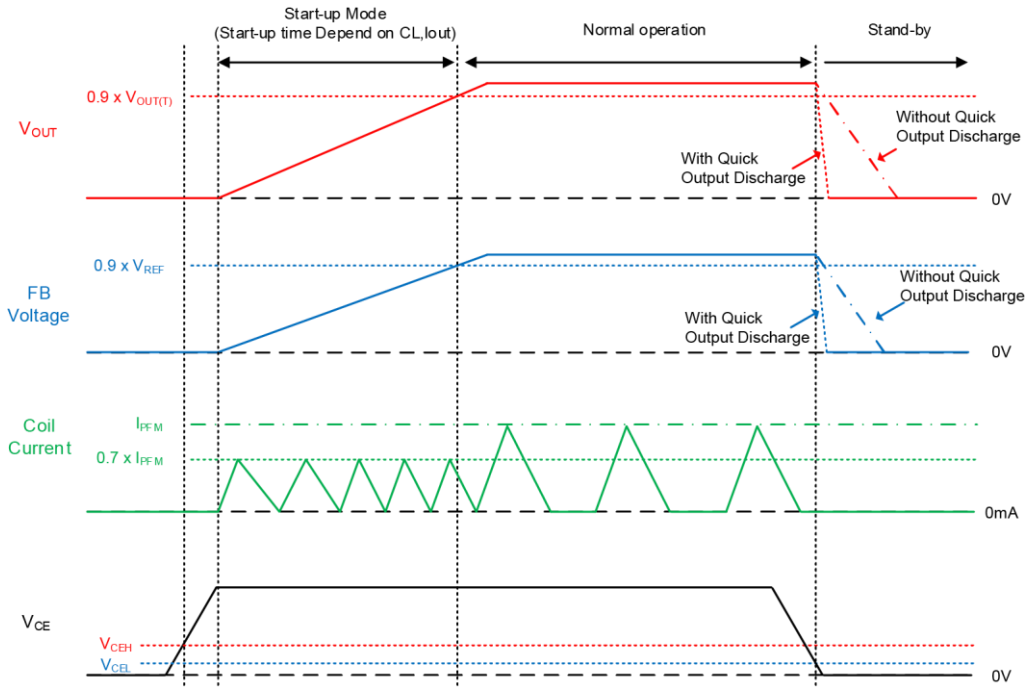
The SNJ conditioner dramatically enhances the quality of the feedback voltage V_{FB} as described above in the feedback control loop to reduce the noise perturbation in response to load fluctuations as well as to reduce the dislocation in on time (T_{ON}) and off-time (T_{OFF}) timing of the sawtooth ripple waveform.

3.3 Current Limit (I_{PFM})

When the high-side MOSFET switch is turned on, the current sense circuit monitors the current that flows through the high-side MOSFET and I_{PFM} is a variable that defines the current limiting threshold. The high-side MOSFET remains on until the current reaches I_{PFM}.

3.4 Start-up Operation

The start-up operation begins when the CE pin voltage is higher than the threshold V_{CEH} and the UVLO function is released, while the FB voltage rises to 0.9 x V_{REF}. The short-circuit protection is deactivated during the start-up, and the inrush current is suppressed by limiting the coil peak current to 0.7 x I_{PFM}. The rise time of the output voltage depends on the output capacitance and the load current.



3.5 Inrush Current Limit

When the input voltage rises at the beginning state of each switching cycle, the short-circuit protection is deactivated until the FB voltage approaches 0.9 x V_{REF} by the step-down operation. To prevent excessive rush current at this state, the coil current flow is limited by the I_{PFM} and by means of the parasite diode of the Nch MOSFET.

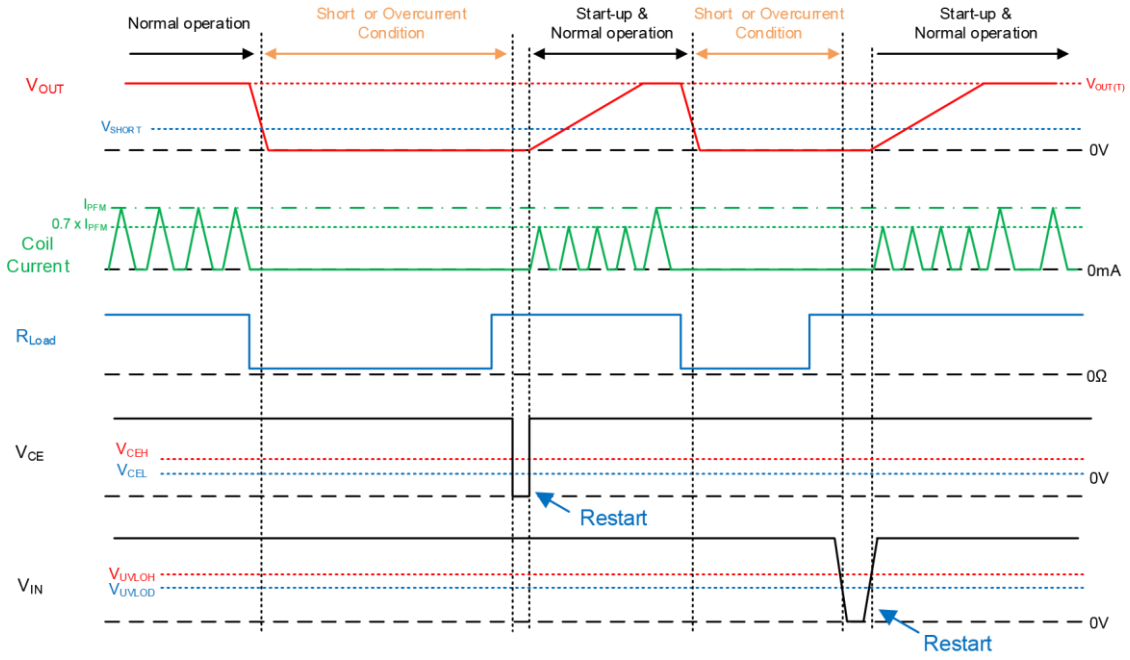
3.6 Enable/Disable

The logic levels of the CE pin is defined by the voltage threshold V_{CEH} and V_{CEL}. A logic high starts the PFM Controller and a logic low disables the PFM Controller to standby mode at which the standby current becomes 0.0 µA.

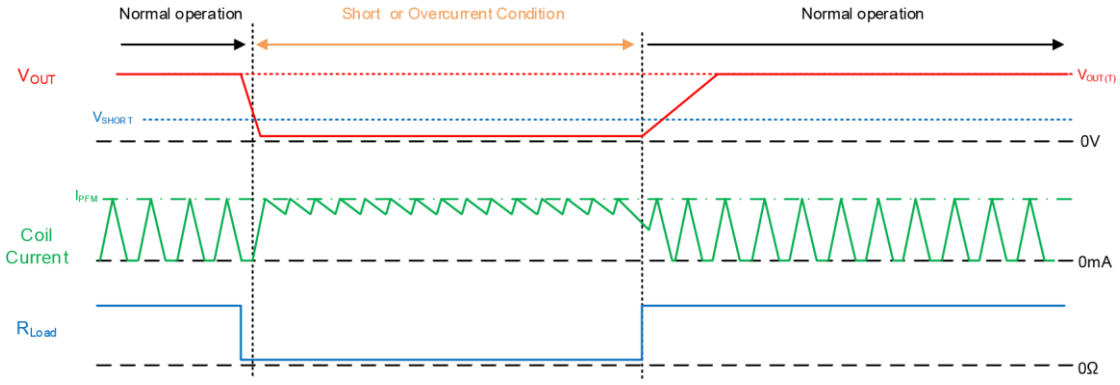
Note: The CE pin requires a prescribed voltage and does not have an internal pull-up or pull-down. If an intermediate voltage is applied to the CE pin, it can cause a through current to flow through the input stage of the CE pin, which can increase current consumption. Therefore, it is important to apply the correct voltage to the CE pin to avoid any issues.

3.7 Short-circuit Protection

For the pre-selected VOUT 1 ≥ 1.2V, when the output voltage V_{OUT} falls below the set short-circuit protection threshold voltage V_{SHORT}, indicating the possibility of a hard short or excessive load current at the output, the high-side Pch MOSFET and low-side Nch MOSFET switches latch. Operation is restarted by reasserting the CE pin, or by reapplying the V_{IN} voltage.



For the pre-selected VOUT 1 < 1.2V, the short-circuit protection function is not operative. If a short circuit or excessive load current occurs, the output voltage will drop and the switching operation will continue. When the short circuit conditions are released, the output voltage rises to the pre-selected output voltage.



3.8 Undervoltage Lockout (UVLO)

The undervoltage lockout circuitry monitors the input voltage level on the V_{IN} pin. When the V_{IN} pin voltage falls below V_{UVLO} (1.4V typ.), the Controller turns off the Pch MOSFET and Nch MOSFET. After the V_{IN} pin voltage rises above the UVLO release voltage, normal operation is resumed with the start-up operation when the CE pin is logic high.

During the UVLO operation, current consumption increases due to the operation of the protection circuits.

3.9 Input Voltage Bypass (100% Duty Cycle Operation)

When the input voltage approaches the output voltage, the PFM Controller stops switching and enters 100% duty cycle operation such that the high-side MOSFET stays on continuously to connect the output via the inductor to the input. When the input voltage is charged again and approaches the release voltage of UVLO, the Controller restarts switching and regulation.

During the 100% duty cycle operation, current consumption increases due to the bypass operation.

3.10 Quick Output Discharge

The PFM Controller integrates an optional, factory programmable discharge switch. This switch turns on when a logic low is asserted at the CE pin or UVLO is activated, which helps to discharge the output capacitor quickly. This feature prevents the malfunction of the powered circuit because charges remain on the output capacitor when the Controller is disabled.

3.11 Switchable Output Voltage Selection

The logic levels of the VSEL pin is defined by the voltage threshold V_{SEL_H} and V_{SEL_L}. For VOUT 2 ≥ 0.6V, a logic high set the output voltage to the pre-selected VOUT 2, and a logic low set the output voltage to the pre-selected VOUT 1, at where VOUT 1 < VOUT 2.

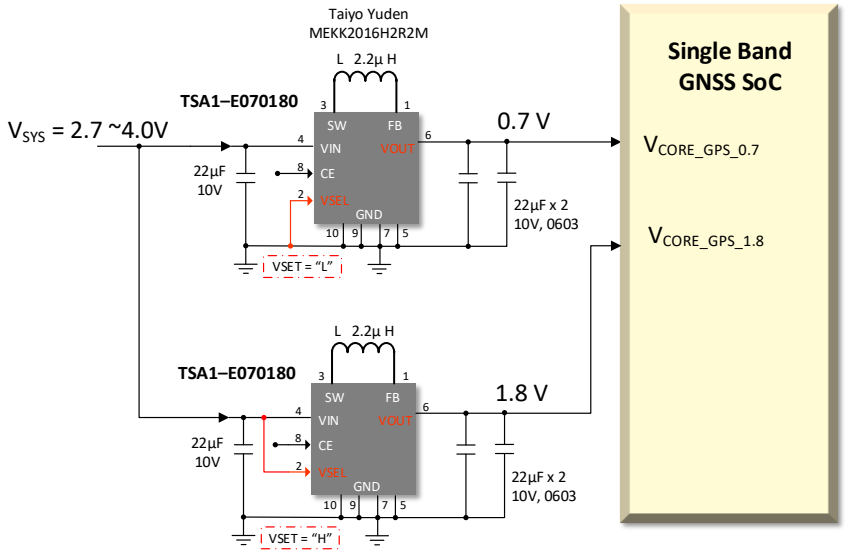
For VOUT 2 = 0.5V, a logic high is set for the 0.5V output, while a logic low is set for VOUT 1 ≥ 0.6V.

Function	Signal	Status
For VOUT 2 ≥ 0.6V: VOUT 1 < VOUT 2		
VSEL	L	VOUT 1
	H	VOUT 2
Note 1: When the logic of VSEL is changed from H -> L or vice versa, the output voltage changes from VOUT 2 to VOUT 1 or vice versa in about 30µs that the transition time depends on the load current and I_{PFM} respectively.		
For VOUT 2 = 0.5V		
VSEL	L	VOUT 1
	H	0.5V
Note 2: When the pre-selected VOUT 2 = 0.5V, a logic low of VSEL changes the output voltage to a higher pre-selected voltage set by the VOUT 1 from 0.6V and above.		

Note: The VSEL pin requires a prescribed voltage and does not have an internal pull-up or pull-down. If an intermediate voltage is applied to the VSEL pin, it can cause a through current to flow through the input stage of the VSEL pin, which can increase current consumption. Therefore, it is important to apply the correct voltage to the VSEL pin to avoid any issues.

4.0 Applications Information

4.1 GNSS Receivers with Dual-voltage Core Rails and Other Noise-sensitive Applications

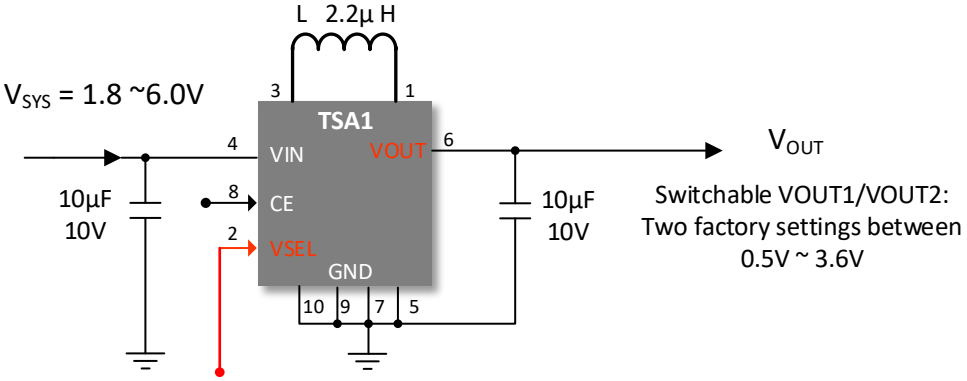


The application circuit above is typically used for GNSS SoCs with a dual-voltage core. The example is also applicable to any other low-power noise-sensitive wireless, mixed signals, and digital SOCs. The selection of components depends on the trade-offs among performance parameters, such as ripple-voltage, spectral noise density, efficiency, and transient response. Varying external components' choice is possible; for example, output capacitor C_{OUT} may be eliminated or added according to different scenarios.

4.2 Versatile for Costs Effective Inventory Management

Empowered by the industry's best 200nA NanoPower architecture and the advantages of low-frequency switching, the Symphony A1 is suitable for all low-power low-voltage applications, especially for those with 1.8V input and below 1V VDD core. The switchable VOUT1/VOUT2 improves inventory management efficiency. Only one part is stocked for two sub-circuits rather than stocking and paying two different parts when one or the other could be excessive or shortage in inventory - it means significant costs saving for sourcing and mass production.

Stock One Part, Use Two Ways.
TSA1- x xxx xxx



4.3 Selecting the Inductor

The DC resistance (DCR) value of the inductor significantly impacts efficiency due to copper losses. Small size inductors tend to have higher DCR, which should be carefully selected. The suggested inductors shown in the table provide a balance between size and DCR.

A minimum requirement of the inductor current rating is for it to provide maximum load current plus half of the inductor current ripple ΔI_L as follows:

$$I_{L(MAX)} = I_{LOAD\,(MAX)} + \left(\frac{\Delta I_L}{2}\right)$$

$$\Delta I_L = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f}\right)$$

$I_{L(MAX)}$ = Maximum inductor current
ΔI_L= Peak-to-peak inductor ripple current
$I_{LOAD(MAX)}$ = Maximum DC Load Current
f = Switching frequency
L = Inductor Value
V_{OUT} = Output voltage
V_{IN} = Input voltage

Recommended Inductors					
Vendor	**Model**	**Inductance (µH)**	**Dimensions (mm)**	**DCR (mΩ)**	**I_{SAT} (mA)**
Alps Alpine	GLUHK2R201A	2.2	2.0 x 1.6 x 1.0		
Taiyo Yuden	MEKK2016H2R2M		2.0 x 1.6 x 0.8		
Sunlord	MWTC201608S2R2MT		2.0 x 1.6 x 0.8		
Murata	DFE18SBN2R2MELL		1.6 x 0.8 x 0.8		
Murata	DFE252010F-2R2M		2.5 x 2.0 x 1.0		
TDK	MLP2520V2R2MT0S1		2.5 x 2.0 x 1.0		

4.4 Selecting the Input Capacitor

A low ESR X7R or X5R ceramic capacitor is required to minimize the input voltage ripple. Although a 10µF capacitor is generally sufficient for nearly all combinations of input current and output voltage, it is essential to account for the loss of capacitance due to the input capacitor's DC bias characteristics. When small 0603 and 0402 case sizes are used, 10V or higher rated voltage is recommended with a 22µF input capacitor, especially for GPS application.

Ceramic capacitors are recommended for input capacitors because of their low equivalent series resistance (ESR) and high ripple current capabilities. The following table shows the recommended input capacitors.

Vendor	Model	Rated Voltage [V]	Capacitance (µF)	Case Size	Dimensions (mm)
Taiyo Yuden	LDK105EBJ226MV-F	10	22	0402	1.0 x 0.5 x 0.5
Taiyo Yuden	LMK107BBJ226MA-T	10	22	0603	1.6 x 0.8 x 0.8
TDK	C1608X5R1A226M	10	22	0603	1.6 x 0.8 x 0.8
TDK	C1608X5R1C106M	16	10	0603	1.6 x 0.8 x 0.8
Taiyo Yuden	EMK107BBJ106MA-T	16	10	0603	1.6 x 0.8 x 0.8
Wurth	885012107014	16	10	0805	2.0 x 1.25 x 1.25

4.5 Selecting the Output Capacitor

The Symphony B2 chipset has proven stability and can supply a power distribution network (PDN) or as a Point-Of-Load (POL) regulator without requiring additional output capacitance. The effect of SNJ conditioning by the HX1 chip is to reduce the influence of output voltage ripple. This means that conventionally specified ripple voltage requirements in mVpp for a given noise-sensitive application may be relieved, enabling the use of more cost-effective output capacitance solutions. For GPS applications, two 22 µF 10V in parallel or one 47 µF 10V is suggested. Early sanity testing helps to evaluate how much output voltage ripple suppression is sufficient. Adding ceramic output capacitors with low ESR, such as X5R or X7R, produce lower output voltage ripple and spectral noise density at low frequencies. Do not use Y5V or Z5U capacitors due to their large capacitance variation over temperature and DC bias. The output capacitors shown in the following table are suggested:

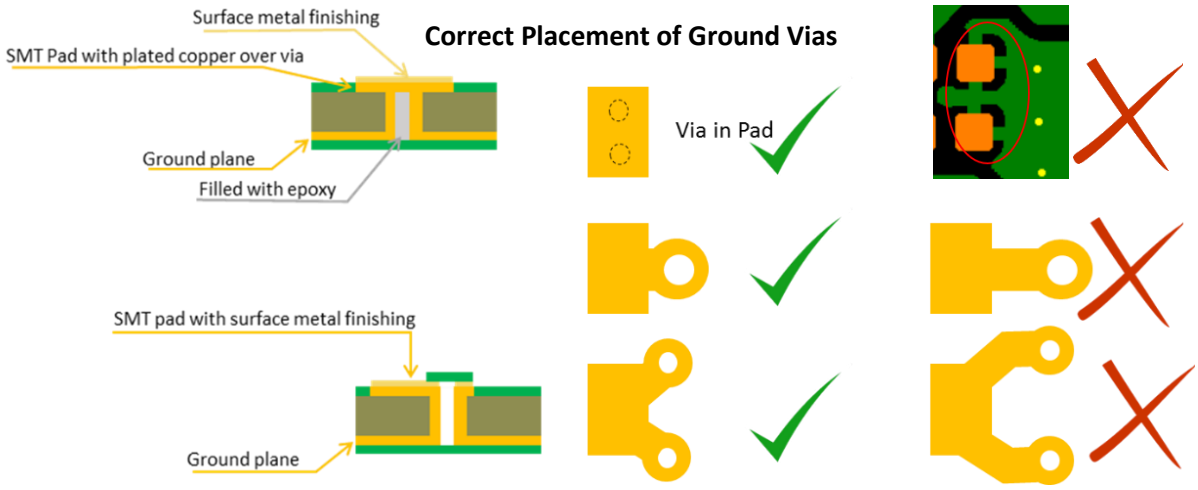
Vendor	Model	Rated Voltage [V]	Capacitance (µF)	Case Size	Dimensions (mm)
Murata	GRM188R60J476ME15J	6.3	47	0603	1.6 x 0.8 x 0.8
AVX	06036D476MAT2A	6.3	47	0603	1.6 x 0.8 x 0.8
Taiyo Yuden	LMK212BBJ476MG-T	10	47	0805	2.0 x 1.25 x 1.25
TDK	C2012X5R1A476M	10	47	0805	2.0 x 1.25 x 1.25
Taiyo Yuden	LDK105EBJ226MV-F	10	22	0402	1.0 x 0.5 x 0.5
Taiyo Yuden	LMK107BBJ226MA-T	10	22	0603	1.6 x 0.8 x 0.8
TDK	C1608X5R1A226M	10	22	0603	1.6 x 0.8 x 0.8
Wurth	885012107011	10	22	0805	2.0 x 1.25 x 1.20

If a large placement separation between the Symphony B2 chipset and the load is required, such as the Symphony chipset placed close to a power source and the load placed close to an antenna, placing additional capacitors, such as 10µF and 0.1µF, at the middle of the trace and close to the input of the load is a remedy to eliminate ringing.

4.6 Layout Guidelines

PCB layout is of utmost importance to avoid potential performance, stability and parasitic problems. Key notes on layout are listed as follows:

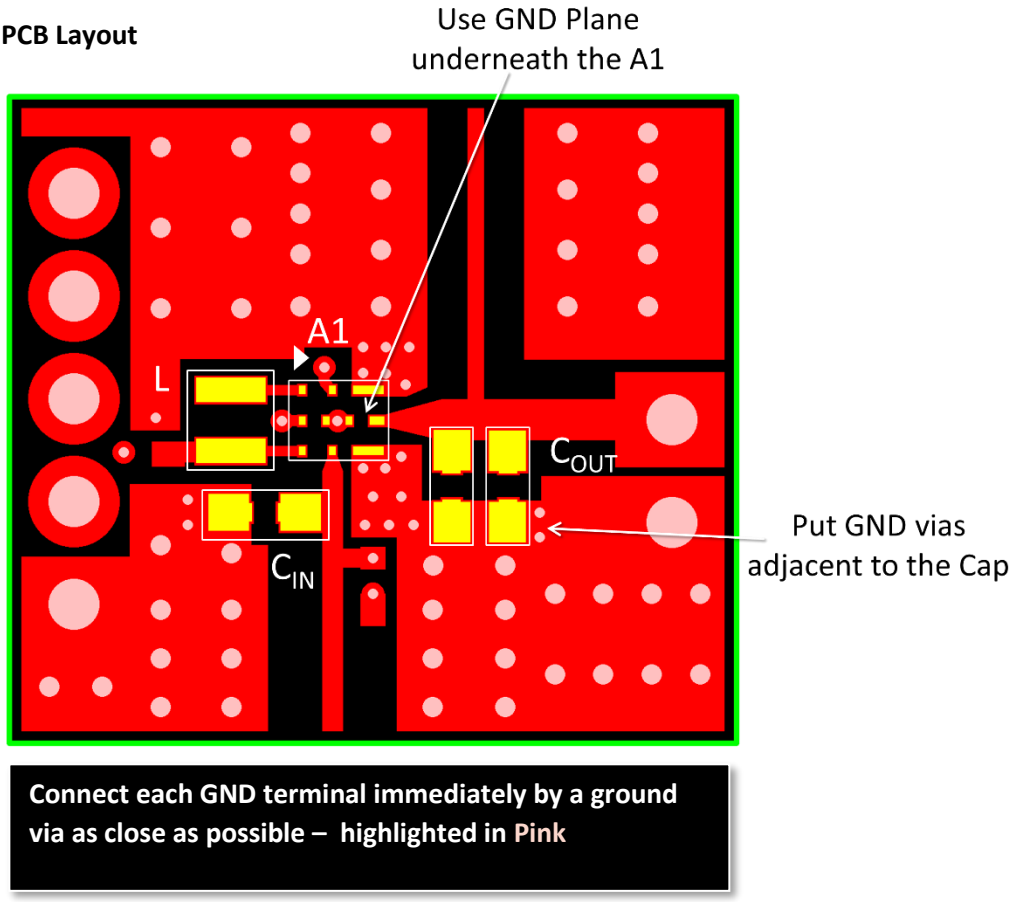
1. **Ground Plane** – use a ground plane in the inner layer immediately below the chipset and connect each GND terminals directly to the ground plane by ground vias. 6 mil (152.4 µm) mechanical drill holes for the ground vias is adequate and must be placed immediately adjacent to the ground terminals as shown in the pictures above. At least one ground via at each end of the GND terminals should be used. Do not use long trace and thermal reliefs to connect the GND terminals. The ground plane should be directly connected to a battery or power source using as wide and as short a connection as possible.
2. **Stitching Vias** – ground planes between different layers should be interconnected with as many stitching ground vias in close proximity as possible. Do not use a single via or vias with large separation to connect different layers of ground planes.
3. **Via-in-Pad** – for compact design, using via-in-pad for connecting all the GND terminals is highly recommended.
4. **Laser Drill** – because the typical diameter of a laser drill via is 50 µm or less, use multiple laser vias but not one in each of the ground terminals.
5. **Signal and Power Traces** – don't run signal and power traces under or in the inner layer below the Symphony A1 without a ground plane inserted in between.
6. **Power Inductor** – place the A1 chip in close proximity to the power inductor and feedback node with traces as wide and as short as possible. Do not route traces under the power inductor.
7. **Input Capacitor** – keep the input capacitor as close as possible to the A1 chip.



4.7 Example of PCB Layout

The following illustrates a 4-layer board that the layer 2 (inner layer 1) must be a ground plane. Good ground planes and grounding vias are essential. Each of the ground terminals should be immediately connected to a ground plane underneath by grounding vias in close proximity (or via-in-pad) - highlighted in pink color as follows.

Example:
Symphony A1 PCB Layout

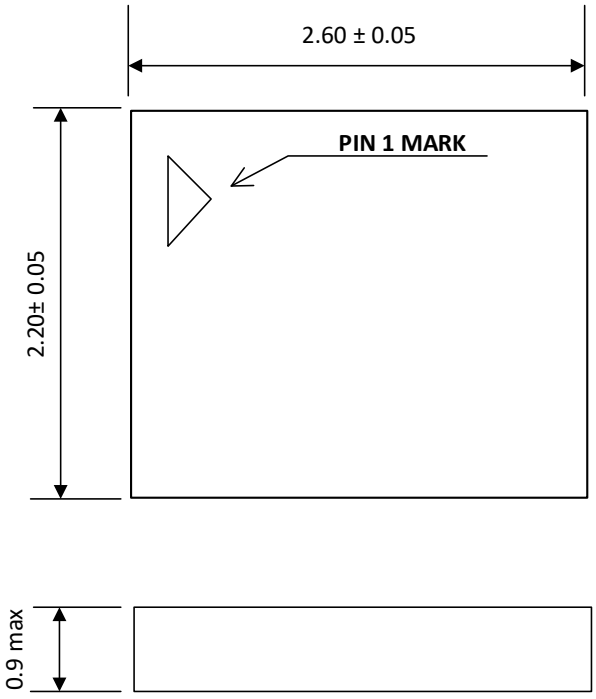


Connect each GND terminal immediately by a ground via as close as possible – highlighted in Pink

5.0 Package and PCB Land Pattern Information

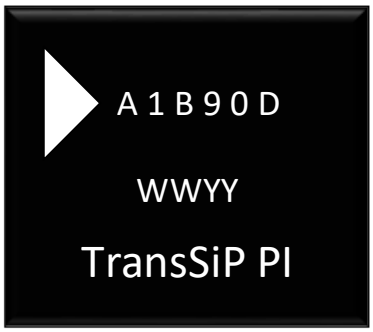
Unit: mm

Symphony A1 LGA-2226
(Top View)



Marking

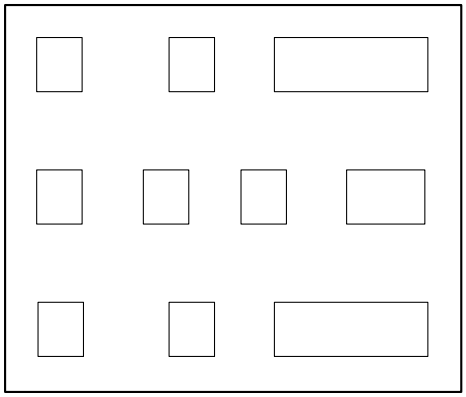
(Illustration Only)



1st Row, part identifier (part dependent)

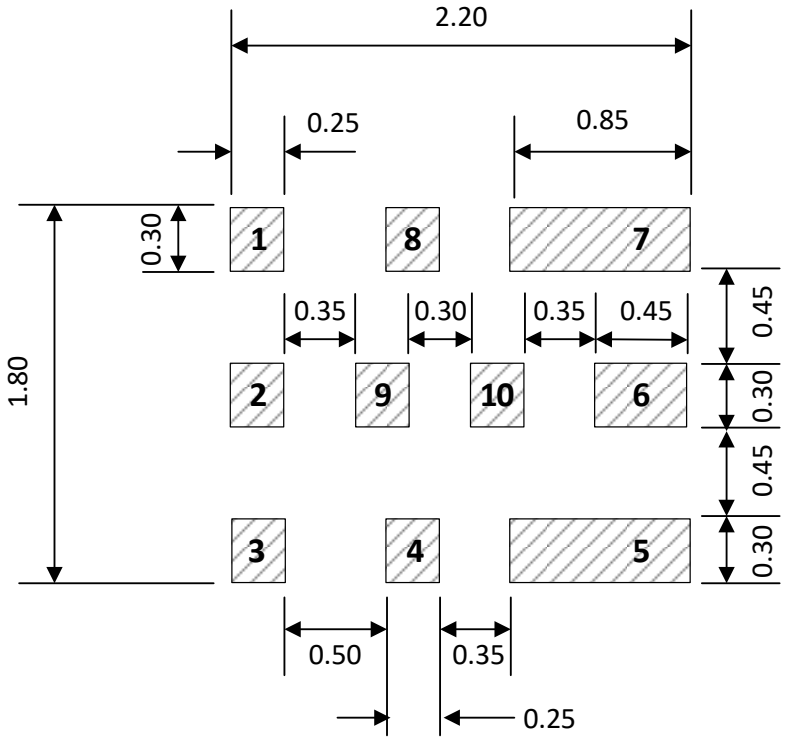
2nd Row, Date Code: Week No. Year

(Bottom View)



Unit: mm

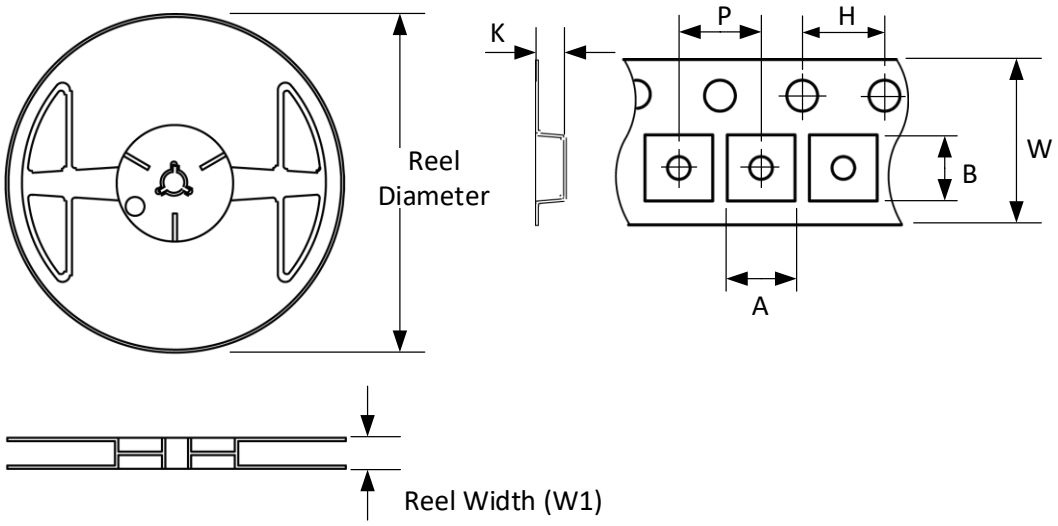
LGA-2226 PCB Land Pattern (Top View)



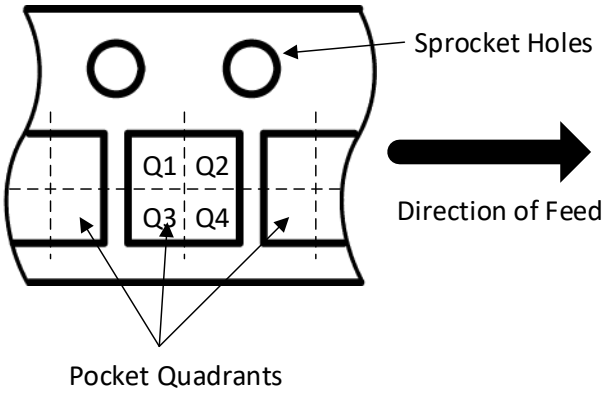
6.0 Tape and Reel Information

Reel Dimensions

Tape Dimensions



Quadrant Assignments for Pin 1 Orientation in Tape



Device	Package Type	Pins	Pin 1 Quadrant	Reel Diameter	Reel Width W1	A	B	K	P	H	W	Qty/ Reel
TSA1	LGA-2226	10	TBD	180	14.0	2.4	2.8	1.05	4.0	4.0	12.0	3000

7.0 Handling and Soldering

7.1 ESD

The Symphony chipset is an electrostatic discharge sensitive device and should be handled in accordance with JESD625-A requirements for Handling Electrostatic Discharge Sensitive (ESDS) Devices. The expecting handling of the Symphony chipset during assembly and test is identical to that of a semiconductor device.

7.2 Moisture Sensitivity Level (MSL) Handling at PCB Assembly

The Symphony A1 is moisture sensitive and is rated as MSL 2a and needs to be handled with proper MSL 2a guidelines to avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation.

MSL 2a devices are dry-packed before shipment from TransSiP. The packing uses a Moisture Barrier Bag (MBB). A Humidity Indicator Card (HIC) and drying desiccant are included the MBB. Shelf life of devices in a sealed bag is 12 months at <40°C and <90% room humidity (RH).

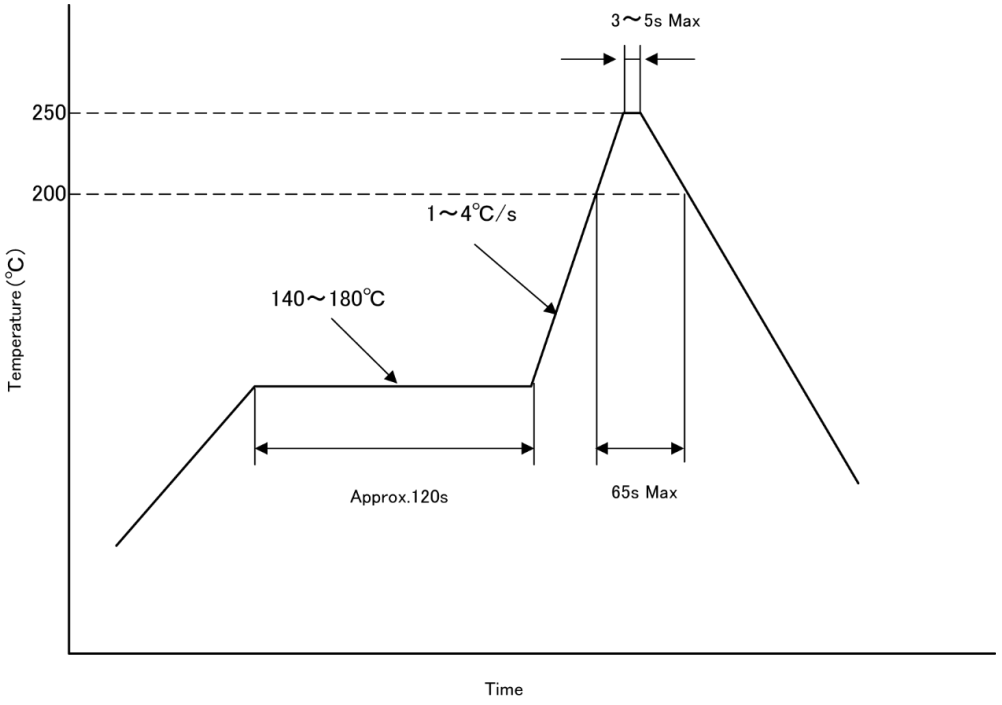
Upon opening of MBB, the HIC should be checked immediately; devices require baking before board mounting if the HIC is >10% when read at 23°C ±5°C.

After MBB is opened, devices should go through reflow for board assembly within 4 weeks at factory conditions of <30°C/60% RH, or stored at <10% RH. If both of these conditions are not met, baking is required before board mounting.

If baking is required, devices should be baked for a minimum of 9 days at 40°C, ≤5% RH.

7.3 Reflow

The Symphony chipset is compatible with lead free soldering processes as defined in IPC/JEDEC J-STD-020. The reflow profile must not exceed the profile given IPC/JEDEC J-STD-020 Table 5-2, “Classification Reflow Profiles”.



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